Erich Viebrock

ECPE 174

**Pre Lab #8**

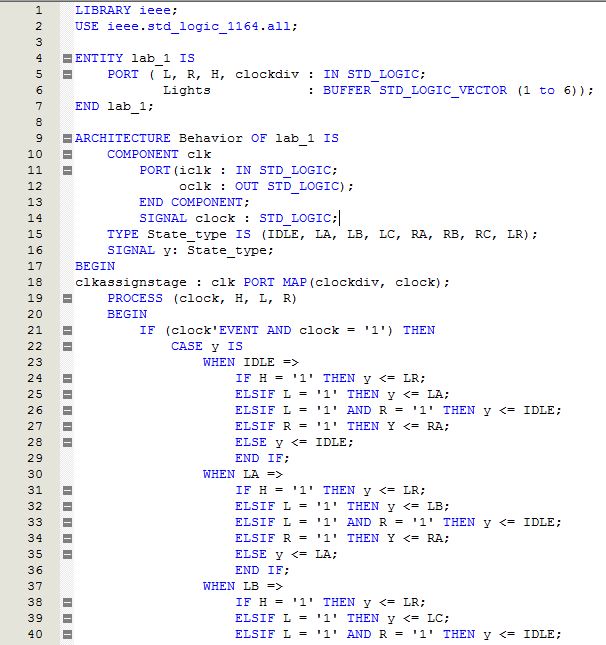
Purpose:

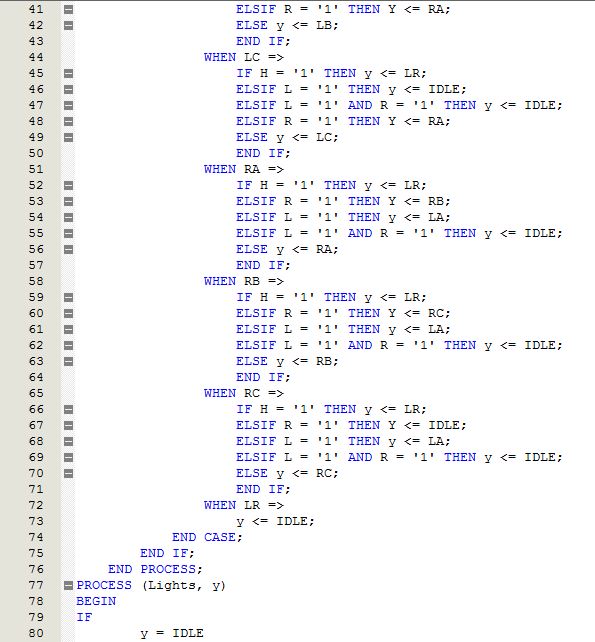
The purpose of this lab is to provide an introduction of Verilog to students. Verilog is very similar to VHDL, has advantages and disadvantages when comparing the two. For most cases, both languages can be used to implement nearly any project, but it is the designer’s choice which language he/she prefers.

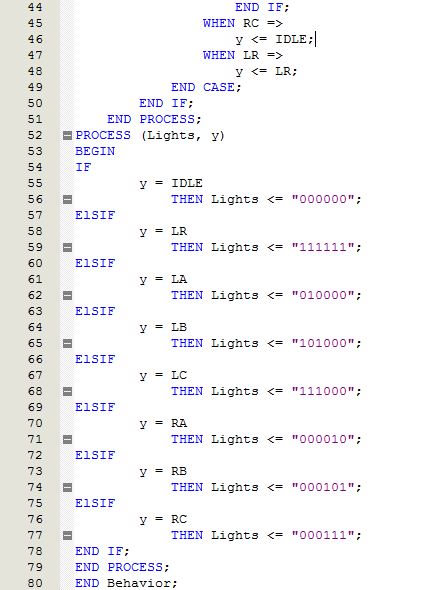
Problem Description:

An old car has tail lights controlled by 6 LEDs. In order to understand which LED is which, the names LA, LB, LC, RA, RB, and RC are used to represent each LED, from left to right. When the car is in IDLE (no switches used), all LEDs should be off. For the switch LEFT, the LEDs flash in a particular order: LB, LA and LC, all left LEDs on, and all off. For the switch RIGHT, the LEDs flash in a particular order: RB, RA and RC, all right LEDs on, and all off. In order to signify HAZARD lights are on, all LEDs flash on, and all LEDs flash off. When LEFT and RIGHT are both turned on, LEDs will go to IDLE. When more than one switch is used and HAZARD is involved, the sequence for HAZARD will begin. For all situations, LEDs will repeat their respected loop until the switch is changed. A clock divider is used in order to display LEDs at a rate conceivable to the human eye. The design is done in a Moore FSM.

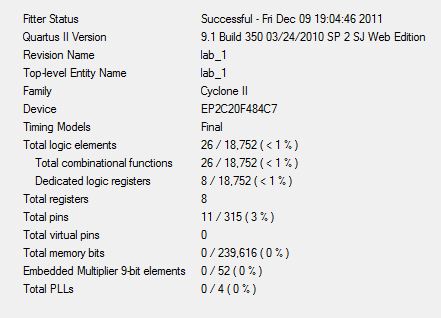
VHDL:



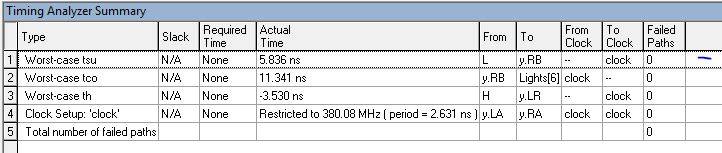




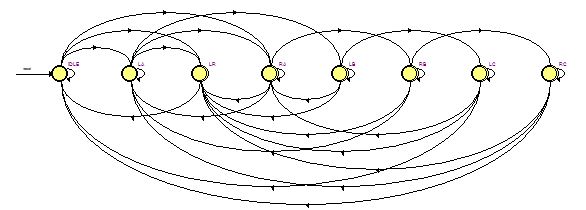
VHDL Fitter Summary:



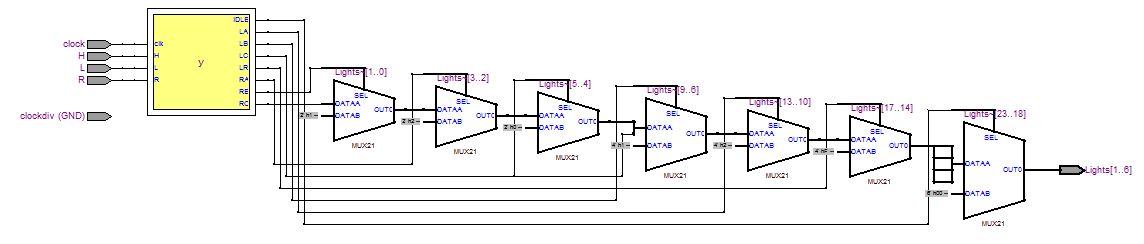
VHDL Timing Summary:



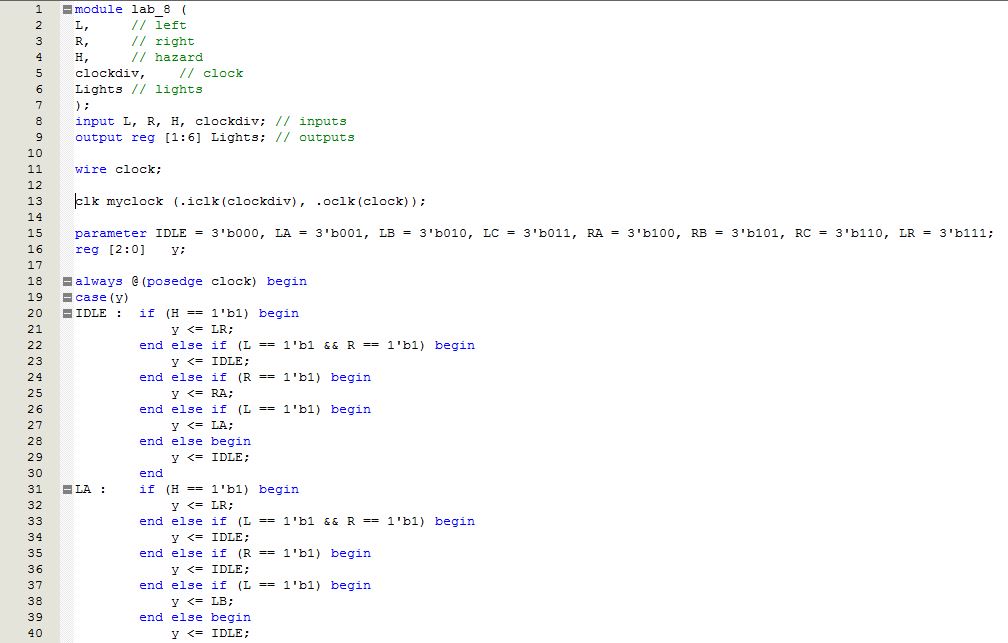
VHDL State Diagram:

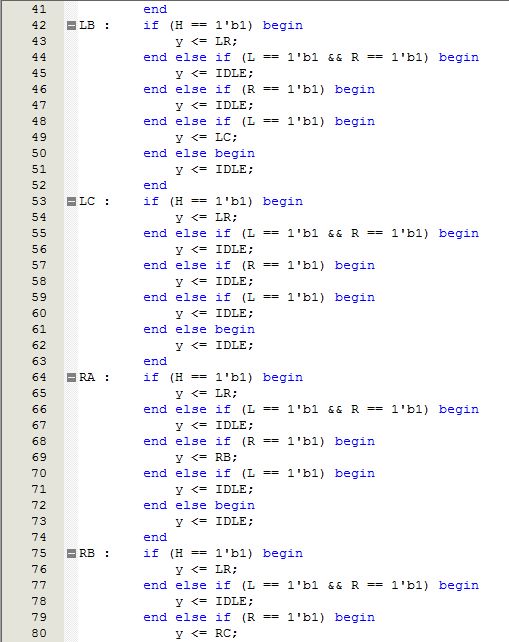


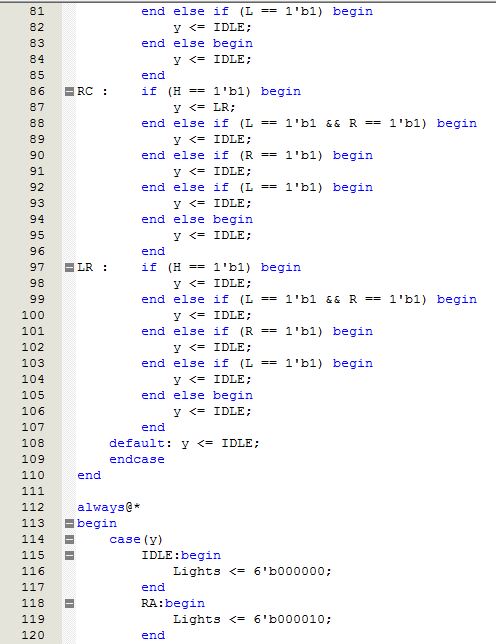
High-Level RTL:

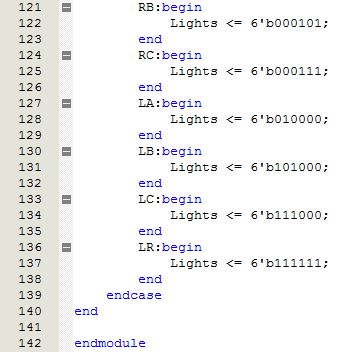


Verilog:

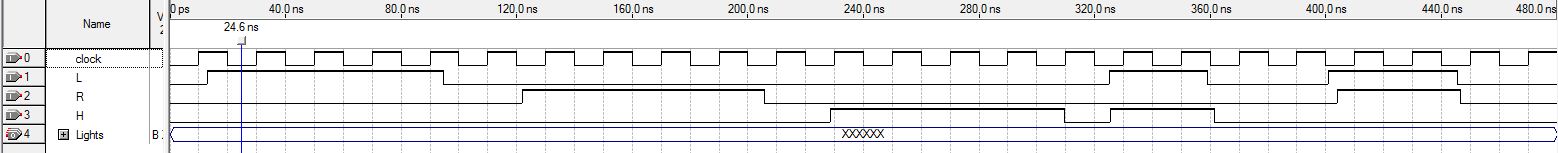




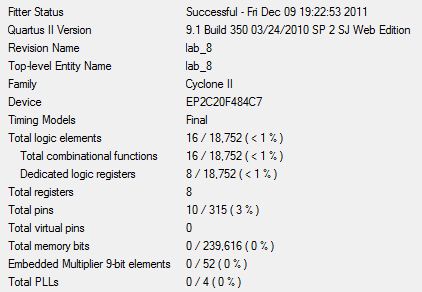




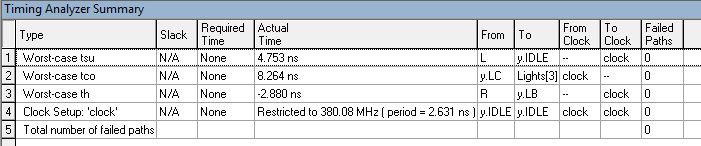
Verilog Simulation:



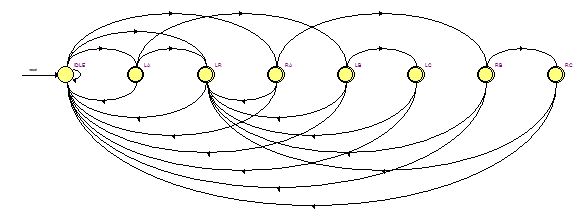
Verilog Fitter Summary:



Timing Summary:



Verilog State Diagram:



Verilog RTL:

